

# SN5430, SN54LS30, SN54S30 SN7430, SN74LS30, SN74S30 8-INPUT POSITIVE-NAND GATES

SDLS099 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

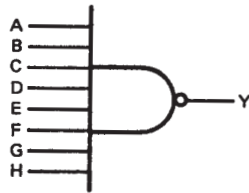
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military range of -55°C to 125°C. The SN7430, SN74LS30, and SN74S30 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

## logic diagram

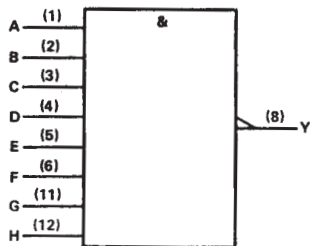


## positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

## logic symbol†

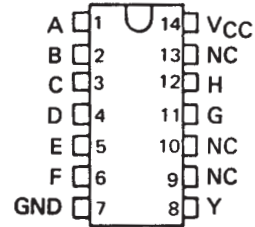


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

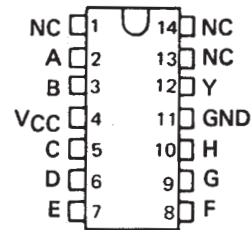
SN5430 . . . J PACKAGE  
SN54LS30, SN54S30 . . . J OR W PACKAGE  
SN7430 . . . N PACKAGE  
SN74LS30, SN74S30 . . . D OR N PACKAGE

(TOP VIEW)



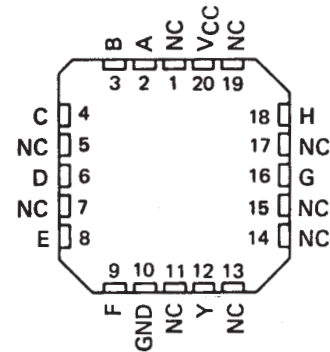
SN5430 . . . W PACKAGE

(TOP VIEW)



SN54LS30, SN54S30 . . . FK PACKAGE

(TOP VIEW)

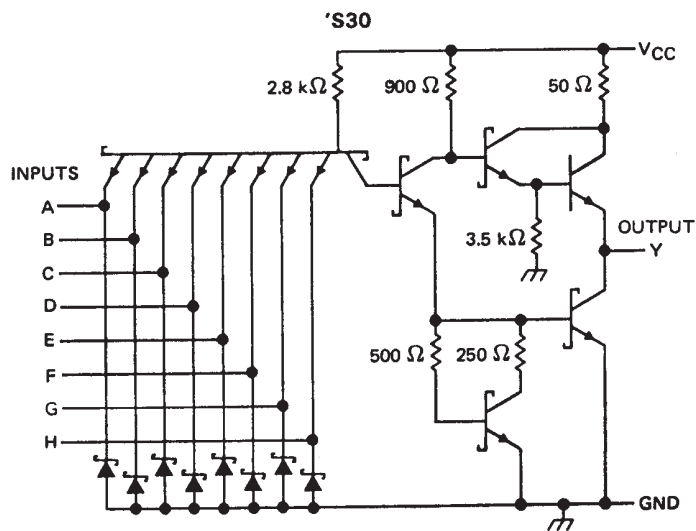
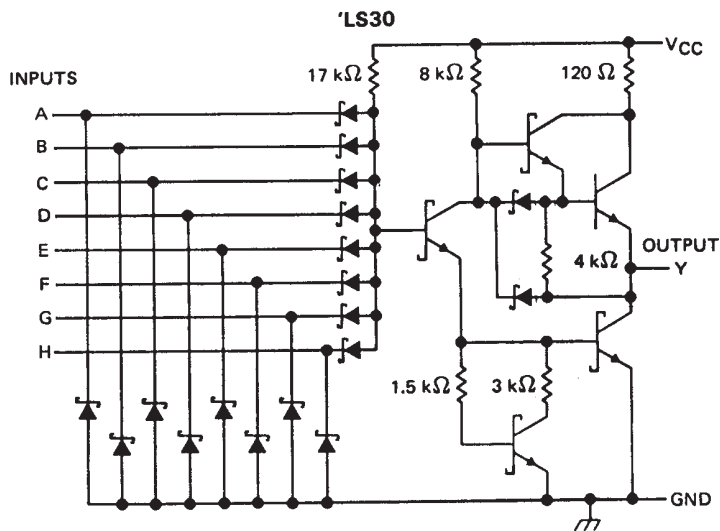
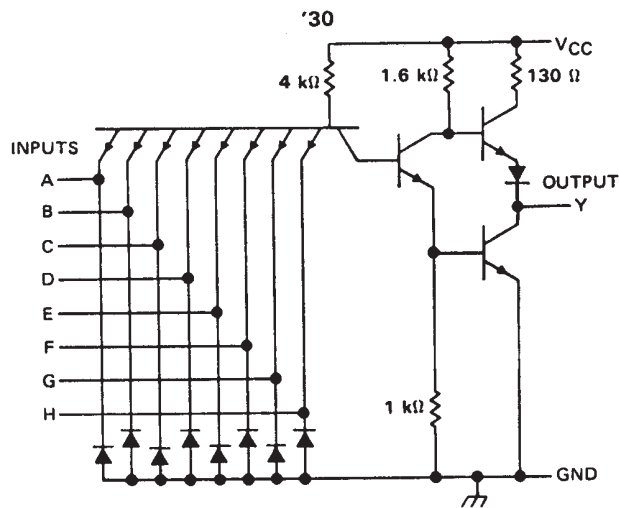


NC - No internal connection

**SN5430, SN54LS30, SN54S30**  
**SN7430, SN74LS30, SN74S30**  
**8-INPUT POSITIVE-NAND GATES**

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**schematics (each gate)**



Resistor values shown are nominal.



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**SN5430, SN54LS30, SN54S30**  
**SN7430, SN74LS30, SN74S30**  
**8-INPUT POSITIVE-NAND GATES**  
SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature range: SN5430 .....	–55 °C to 125 °C
SN7430 .....	0 °C to 70 °C
Storage temperature range .....	–65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

	SN5430			SN7430			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			–0.4			–0.4	mA
$I_{OL}$ Low-level output current			16			16	mA
$T_A$ Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN5430			SN7430			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–1.6			–1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	–20		–55	–18		–55	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		1	2		1	2	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		3	6		3	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		13	22	ns
$t_{PHL}$					8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**SN5430, SN54LS30, SN54S30**  
**SN7430, SN74LS30, SN74S30**  
**8-INPUT POSITIVE-NAND GATES**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	7 V
Operating free-air temperature range: SN54LS30 .....	-55°C to 125°C
SN74LS30 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

	SN54LS30			SN74LS30			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			-0.4			-0.4	mA
$I_{OL}$ Low-level output current			4			8	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN54LS30			SN74LS30			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4				0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.25	0.5		
$I_I$	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		0.35	0.5		0.35	0.5	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		0.6	1.1		0.6	1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$   
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		8	15	ns
$t_{PHL}$					13	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**SN5430, SN54LS30, SN54S30**  
**SN7430, SN74LS30, SN74S30**  
**8-INPUT POSITIVE-NAND GATES**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature range: SN54S30 .....	–55 °C to 125 °C
SN74S30 .....	0 °C to 70 °C
Storage temperature range .....	–65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

	SN54S30			SN74S30			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			–1			–1	mA
$I_{OL}$ Low-level output current			20			20	mA
$T_A$ Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS †	SN54S30			SN74S30			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.2			–1.2	V
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			–2			–2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	–40		–100	–40		–100	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		3	5		3	5	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		5.5	10		5.5	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		4	6	ns
$t_{PHL}$					4.5	7	ns
$t_{PLH}$			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		5.5		ns
$t_{PHL}$					6.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9679201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9679201QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9679201QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9679201QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9679201QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30009B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30009B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30009BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30009BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30009BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30009BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30009SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30009SCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30009SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/30009SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN5430J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN5430J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN7430N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7430N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS30D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS30DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS30J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS30N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS30N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS30N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS30N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS30NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS30NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS30NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS30NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S30D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S30D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S30DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S30DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S30J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74S30J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74S30N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S30N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ5430J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5430J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5430W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5430W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS30FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS30FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS30W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS30W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54S30FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S30FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SNJ54S30J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S30W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54S30W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS30DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS30NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS30DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS30NSR	SO	NS	14	2000	346.0	346.0	33.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

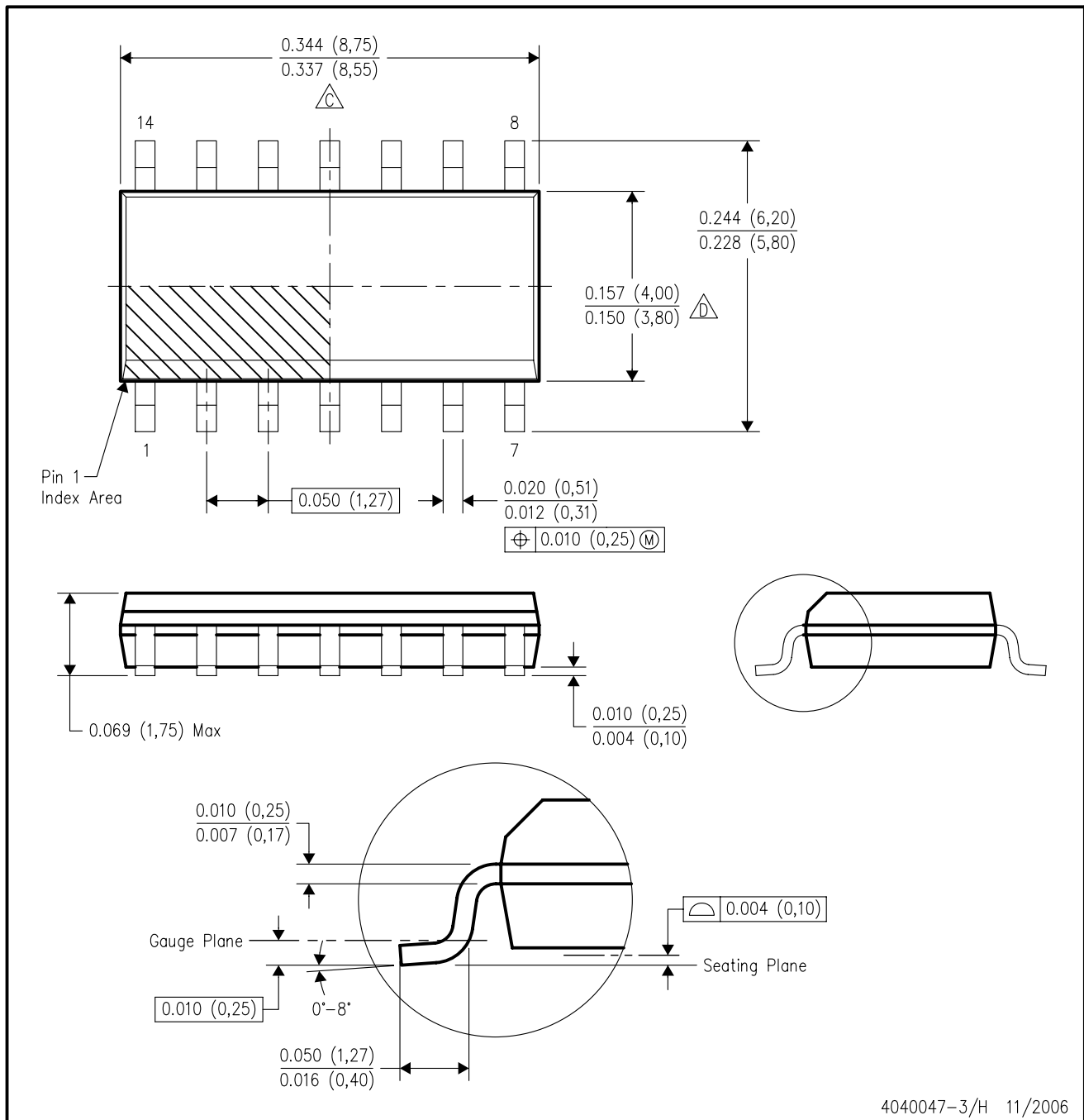
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

D (R-PDSO-G14)

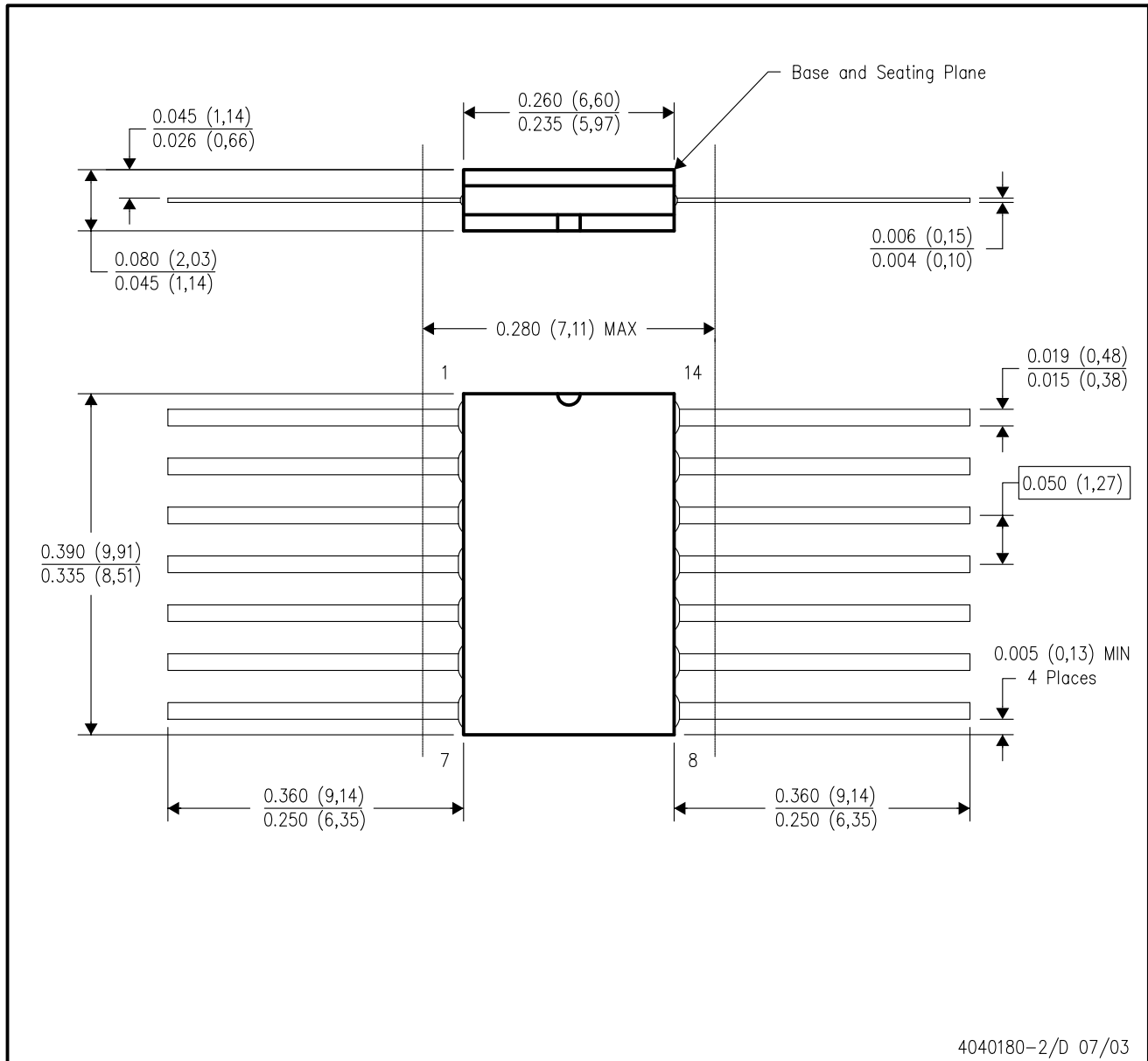
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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